WHAT IS CLAIMED IS:

1. A floating point flag forcing circuit for selectively clearing at least a portion of encoded status flag information within a floating point operand, comprising:

a first circuit that determines a predetermined format associated with the floating point operand from the encoded status flag information within the floating point operand; and

a second circuit that assembles a resulting operand in which at least a portion of the encoded status flag information of the resulting operand is cleared based upon the predetermined format and an assembly signal generated by the first circuit.

2. The floating point flag forcing circuit of claim 1, wherein the first circuit comprises:

an analysis circuit that analyzes the floating point operand and generates an intermediate indication of a bit pattern associated with the floating point operand; and

a decision circuit that receives the intermediate indication from the analysis circuit to determine the predetermined format associated with the floating point operand, the decision circuit also being capable of generating the assembly signal, which is provided to the second circuit.

3. The floating point flag forcing circuit of claim 1, wherein the second circuit assembles the resulting operand by selectively forcing the at least a portion of the encoded status flag information of the resulting operand to a selected value in accordance with a rounding mode signal and the assembly signal.

4. The floating point flag forcing circuit of claim 3, wherein the selected value is based upon the predetermined format of the floating point operand, the control signal, and the rounding mode signal.

5. The floating point flag forcing circuit of claim 1, wherein the encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, an inexact flag, and a division by zero operation flag.

6. The floating point flag forcing circuit of claim 1, wherein the predetermined format represent a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

7. The floating point flag forcing circuit of claim 6, wherein an overflow format represents one of a +OV status and a -OV status.

8. The floating point flag forcing circuit of claim 6, wherein an underflow format represents one of a +UN status and a -UN status.

9. A method for forcing floating point status information for selectively clearing at least a portion of encoded status flag information within a floating point operand, comprising:

receiving the floating point operand;

analyzing the encoded status flag information associated with the floating point operand to identify a predetermined format associated with the floating point operand;

receiving a control signal for selectively clearing the encoded status flag information;

generating an assembly signal; and

assembling a resulting operand in which at least a portion of the encoded status flag information of the resulting operand is cleared based upon the predetermined format and values of the control signal and the assembly signal.

10. The method of claim 9, wherein the step of analyzing further comprises:

generating an intermediate indication of a bit pattern associated with the floating point operand based upon the encoded status flag information for the floating point operand; and

determining the predetermined format associated with the floating point operand based upon the intermediate indication.

11. The method of claim 9, wherein the assembling step further comprises assembling the resulting operand by selectively forcing the at least a portion of the encoded status flag information of the resulting operand to a selected value in accordance with a rounding mode signal and the assembly signal.

12. The method of claim 11, wherein the selected value is based upon the predetermined format of the floating point operand and the value of the control signal and the rounding mode signal.

13. The method of claim 9, wherein the encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, an inexact flag, and a division by zero operation flag.

14. The method of claim 9, wherein the predetermined format represent a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

15. The method of claim 14, wherein an overflow format represents one of a +OV status and a -OV status.

16. The method of claim 14, wherein an underflow format represents one of a +UN status and a -UN status.

17. A computer-readable medium on which is stored a set of instructions for selectively clearing at least a portion of encoded status flag information within a floating point operand, which when executed perform the steps of:

receiving the floating point operand;

analyzing the encoded status flag information associated with the floating point operand to identify a predetermined format associated with the floating point operand;

receiving a control signal for selectively clearing the encoded status flag information;

generating an assembly signal; and

assembling a resulting operand in which at least a portion of the encoded status flag information of the resulting operand is cleared based upon the predetermined format and values of the control signal and the assembly signal.

18. The computer readable medium of claim 17, wherein the step of analyzing further comprises:

generating an intermediate indication of a bit pattern associated with the floating point operand based upon the encoded status flag information for the floating point operand; and

determining the predetermined format associated with the floating point operand based upon the intermediate indication.

19. The computer readable medium of claim 17, wherein the assembling step further comprises assembling the resulting operand by selectively forcing the at least a portion of the encoded status flag information of the resulting operand to a selected value in accordance with a rounding mode signal and the assembly signal.

20. The computer readable medium of claim 19, wherein the selected value is based upon the predetermined format of the floating point operand and the value of the control signal and the rounding mode signal.

21. The computer readable medium of claim 17, wherein the encoded status flag information represents an invalid operation flag, an overflow flag, an underflow flag, an inexact flag, and a division by zero operation flag.

22. The computer readable medium of claim 17, wherein the predetermined format represent a zero format, an overflow format, an underflow format, a denormalized format, a normalized non-zero format, an infinity format, and a not-a-number (NaN) format.

23. The computer readable medium of claim 22, wherein an overflow format represents one of a +OV status and a -OV status.

24. The computer readable medium of claim 22, wherein an underflow format represents one of a +UN status and a -UN status.